USING TRANSITION TIME CHECKS TO DETERMINE NOISE PROBLEMS ON SIGNAL LINES OF AN INTEGRATED CIRCUIT

TECHNICAL FIELD OF THE INVENTION

The present invention is generally related to integrated circuits (ICs) and, more particularly, to using transition times on signal lines in an IC to determine whether the signal lines have potential noise problems associated with them.

BACKGROUND OF THE INVENTION

As the geometries in integrated circuits (ICs) become ever increasingly smaller, the metallic signal lines on the ICs have become smaller in width and the spacing between the signal lines has decreased. This decrease in the width of the signal lines has increased the resistance of the signal lines. In order to reduce the resistance of the signal lines, the signal lines have been increased in height. However, this increase in height coupled with the reduction in the spacing between the signal lines increases the capacitance between adjacent signal lines. A given signal line has a signal line on each side of it, which results in the line in question coupling charge onto the lines on each side of it. Because the spacing between the lines is becoming smaller, the coupling capacitance between the lines is increasing. In addition, charge is also coupled onto the lines by elements on the IC above and below the signal lines.

This capacitance creates concerns because if, for example, the lines on both sides of the line in question are transitioning from high to low, and the line in question is at a high level, the coupling capacitance between the lines can cause the line in question to dip down to some extent below its high level. If the voltage level on the line in question dips down far enough, then the logic gate that is connected to the line in question sees a transition to a low level, which results in an erroneous state.

Various scenarios exist that make such an erroneous transition a concern. In one scenario, if the erroneous transition occurs simultaneously with, or very close in time to the end of the clock period, then the register that is capturing the next state will receive an erroneous state. Another scenario is, if the line in question is transitioning from low to high as the line on either side of it is transitioning low, the transition speed of the line in question will be reduced. If the transition speed is sufficiently reduced, then the timing requirements of the register downstream will not be met, i.e., the setup time of the downstream register will be violated. The setup time is the amount of time before the clock transitions that the data needs to be valid at the input to the register. In another scenario, if the adjacent lines are transitioning in the same direction as the line in question, then the transition speed of the line in question will be increased, which can cause hold time requirements to be violated. The hold time is the amount of time after the clock transitions that the voltage level (i.e., high or low) on the line must remain valid before it changes.

Accordingly, a need exists to be able to determine whether such transitions will result in noise on signal lines that is sufficient to cause setup and/or hold time requirements to be violated or to cause erroneous data to be latched in a register.

SUMMARY OF THE INVENTION

In accordance with the present invention, maximum transition time constraints for drivers of different sizes driving signal lines of respective maximum lengths are compared to signal transition times of an IC design to determine whether a potential noise problem exists with respect to the signal lines. Each driver size has a maximum line length constraint and a corresponding maximum transition time constraint associated with it. These maximum transition time constraints are used to determine whether the signal lines connected to respective drivers in the IC will have potential noise problems associated with them.

In accordance with the preferred embodiment of the present invention, each signal line is checked for potential noise problems. For each signal line in the IC design, the signal transition time is determined and compared to the maximum transition time constraint associated with the size of the driver driving the signal line. If the signal transition time exceeds the maximum transition time constraint, a potential noise problem exists with respect to the signal line.

These and other features and advantages of the present invention will become apparent from the following description, drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating capacitive coupling between adjacent signal lines on an IC.

Fig. 2 is a set of voltage verses time waveforms that demonstrate when the Victim line shown in Fig. 1 exhibits a noise problem and when it does not.

Fig. 3 is a circuit diagram illustrating three lines of different lengths driven by three respective drivers of different sizes.

Fig. 4 is a set of waveforms corresponding to the transitions of the signals on the three lines shown in Fig. 3.

Fig. 5 is a flow chart of the method of the present invention in accordance with the preferred embodiment for identifying signal lines having noise problems associated with them.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with the present invention, simulations were performed during which signal lines on either side of a signal line in question were switched from one state to another and the noise spike on the line in question was measured. It was determined that the size of the noise spike was dependent on the lengths of the lines. In other words, the longer the lengths of the signal lines that run next to each other, the greater the total capacitive coupling, and at some length, the coupling is sufficient to produce enough noise on a given line to cause one of the aforementioned transitioning problems to occur (i.e., erroneous data is latched in a register). The simulation determined the transition times for various line lengths and their respective drivers. Based on the transition times, it can be determined whether a given line is

long enough to cause coupling capacitance to produce enough noise on the line to cause problems.

The potential capacitive coupling problems will now be described with reference to the circuit 1 shown in Fig. 1. Fig. 1 illustrates three adjacent signal lines that are labeled "Aggressor 1", "Victim" and "Aggressor 2". The signal line in question is the Victim line 3. The maximum length of the Victim line 3 is affected by the Aggressor lines 2 and 4. Each of the lines has a resistance associated with it. The resistance associated with line 2 is represented by the resistors 5, 6 and 7. The resistance associated with line 3 is represented by the resistors 8, 9 and 10. The resistance associated with line 4 is represented by the resistors 11, 12 and 13. . Each of the lines has a resistance and capacitance associated with it. Each signal line also has its own fixed capacitance. The capacitance associated with line 2 is represented by the capacitors 14, 15 and 16 connected to ground. The capacitance associated with line 3 is represented by the capacitors 17, 18 and 19 connected to ground. The capacitance associated with line 4 is represented by the capacitors 20, 21 and 22 connected to ground.

As stated above, capacitive coupling between adjacent signal lines also exists. The capacitive coupling between lines 2 and 3 is represented by capacitors 26A, 26B and 26C. The capacitive coupling between lines 3 and 4 is represented by capacitors 27A, 27B and 27C. Therefore, the total capacitance in the circuit 1 is based on the fixed capacitance of the lines, which is represented by capacitors 14 – 22, and the capacitive coupling between the lines, which is represented by capacitors 26A – 26C and 27A – 27C.

Each of the signal lines 2, 3 and 4 has a driver 23, 24 and 25, respectively, associated with it that drives the line. Fig. 2 is a graph 30 illustrating the voltage of the Victim line 3 as a function of the amount of time a signal is propagating along the Victim line 3. Three nodes are labeled on the Victim line 3 at different locations along the Victim line 3. The nodes are labeled A, B and C and represent the maximum length of the line 3 for a given driver size. Fig. 2 illustrates that if a signal is driven on line 3 beyond node B, the noise threshold represented by the dashed line 31 will be exceeded. Therefore, the maximum length of the Victim line 3 for a driver of a given size "X" in this example is the length from the driver 24 to node B. If the voltage on the Victim line 3 is sufficient to drive the signal on the line beyond node B, the downstream logic coupled to Victim line 3 will detect a noise spike, which could result in the detection of an erroneous state by the downstream logic. Of course, for different driver sizes, the maximum permissible line length will be different.

It is known in the art of IC design that, for a driver of a given size, a maximum length line exists that can be driven before a noise issue arises. In accordance with the present invention, simulations were performed for drivers of all sizes driving their respective maximum length lines and it was determined what the respective transition times for all of the different driver sizes and route lengths were. This concept is demonstrated by the circuit diagram 40 of Fig. 3 and by the voltage verses time diagram 50 of Fig. 4.

Fig. 3 illustrates three drivers 41, 42 and 43 of three different sizes, namely sizes A, B and C, respectively. Driver 41 drives a line 44 of maximum length X. Driver 42 drives a line 45 of maximum length Y. Driver 43 drives a line 46 of maximum length Z. The lines 44, 45 and 46 are shown as having respective fixed resistances and capacitances R1/C1, R2/C2 and R3/C3, respectively. The same signal

47 was used during a simulation in accordance with the present invention to simultaneously drive the drivers 41, 42 and 43 and the maximum transition times were measured at the ends 48, 49 and 50 of the lines. Although the lines 44, 45 and 46 are illustrated as being of the same length, they are not. The lengths X, Y and Z are different for the different drivers 41, 42 and 43, respectively. Also, in actuality, the simulation involved many more drivers and lines, but only three are shown for ease of illustration.

The capacitive coupling between the lines was not taken into consideration because each of the lines was being driven by the same signal 47 in the same direction at the same time. In accordance with the present invention, it was determined that these maximum transition times for each driver and its corresponding maximum length line can be used as threshold values to determine if a capacitive coupling problem or, more generally, a noise problem, exists. Therefore, the present invention enables lines that may have capacitive coupling problems associated with them to be identified without the need for performing a coupling capacitance simulation on each and every line in the design.

In essence, in accordance with the present invention, if the transition time on a signal line is determined to be less than or equal to the maximum transition time for the driver size and its corresponding maximum line length, no noise issues (i.e., capacitive coupling problems) need to be addressed. If the transition time exceeds the maximum transition time for the driver, then a noise problem resulting from capacitive coupling is determined to exist and steps will need to be taken to eliminate the problem. The manner in which the problem is eliminated is outside of the scope of the present invention. Such problems may be rectified by, for example, shortening the line length or interrupting the line with a repeater.

The method 60 of the present invention in accordance with the preferred embodiment is shown in Fig. 5. As stated above, a simulation was performed for each driver size and its associated maximum line length to determine the maximum transition time for each driver. This simulation is represented by block 61. Preferably, this simulation is only performed once for a given IC fabrication process. The results preferably are stored in a table that associates each driver size with a maximum transition time.

With this information, each line of a design can be tested to determine whether the line has a noise problem associated with it. As indicated in block 63, a determination is made as to whether or not the maximum transition time has been exceeded for the given driver. If so, a determination is made that a capacitive coupling problem exists, as indicated by the arrow from block 63 to block 66. If a determination is made at block 63 that the maximum transition time has not been exceeded, then a determination is made that there is no noise problem associated with the signal line, as indicated by the arrow from block 63 to block 65.

Another advantage of the present invention is that it allows the number of noise problems in synthesized blocks to be reduced. By looking at the range of maximum transition times, a transition time can be chosen that corresponds to the minimum transition time found in that range and used as a maximum transition time constraint in synthesis. This is especially useful when using Physical Synthesis where the tool will then place cells close enough together to prevent exceeding this maximum transition time constraint, or the tool will insert a buffer in the corresponding route. Thus, noise problems can be prevented a priori.

It should be noted that the present invention has been described with reference to the particular embodiments and that modifications to the embodiments described herein can be made without deviating from the scope of the present invention. It should also be noted that the present invention is not limited to any particular IC process. For example, the present invention applies to field effect transistor (FET) technology as well as bipolar junction transistor technology (BJT) or any other IC process technology currently in use or developed in the future.